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Hardware Implementation of Multilevel DC-Link Inverter Supplying Resistive Load

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ABSTRACT: This paper presents hardware implementation of the nine level cascaded H-bridge multilevel inverter based on a multilevel DC link (MLDCL) and a bridge inverter with efficient switching sequence to reduce the number of switches thereby reducing the switching losses and device stresses. Compared to existing Multilevel inverters such as diode clamped & flying capacitor inverters the proposed cascaded H-bridge multilevel DC-link inverter requires least no of switches to achieve same no of voltage levels. Optimized circuit layout is possible because each level have same structure and there is no extra clamping diodes or capacitors. The MLDCL provides a DC voltage with the shape of a staircase and it is given to the bridge inverter, which in turn alternates the polarity to produce an AC voltage. Compared with the existing type of cascaded H-bridge multilevel inverter, the MLDCL inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. For a given number of voltage levels, the required number of active switches is 2 (m-1) for the existing multilevel inverters, but it is m+3 for the MLDCL inverters. The Hardware is implemented using ATMEL 89C51 microcontrollerfor suppyling resistive load.

KEYWORDS: Cascaded half bridge, multilevel dc link, multilevel inverter, reduced component count, switching sequences.

I. INTRODUCTION

The voltage source inverters produce an output voltage or current with levels either 0 or $\pm V_{dc}$. They are known as the two-level inverter. To produce a quality output voltage or a current wave form with less amount of ripple content, they require high switching frequency. In high- power and high-voltage applications these two level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings [1]. These limitations can be overcome using multilevel inverters. The multilevel inverters have drawn tremendous interest in power industry.It may be easier to produce a high-power, high-voltage inverter with multi level structure because of the way in which the voltage stresses are controlled in the structure[3].

The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without use of transformers or series connected synchronized-switching devices. As the number of voltage levels increases, the harmonic content of the output voltage wave form decreases significantly. There are 3 types of multilevel inverters named as diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter. These three types of multilevel inverters requires more no of components such as switches, clamping diodes and capacitors [10]. As the number of voltage levels m grows the number of active switches increases according to 2×(m-1**)** for the cascaded H-bridge multilevel inverters.

II.CASCADED H-BRIDGE MLDCL INVERTER TOPOLOGY

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Figure.1 shows a block diagram of the presented cascaded H-bridge MLDCL inverter topology, which consists of a multilevel DC source to produce DC-link bus voltage V_{bus} and a single-phase full-bridge (SPFB) inverter consists of four switches S1-S4 to alternate polarity of DC-link bus voltage to produce an AC voltage. The DC source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two switches S_{ak} and S_{bk}. The two switches and operate in a toggle fashion [1]. The cell source is bypassed with S_{ak} on and S_{bk} off, or adds to the dc-link voltage by reversing the switches. Figure.2 shows a circuit diagram of the presented cascaded H-bridge MLDCL inverter topology.

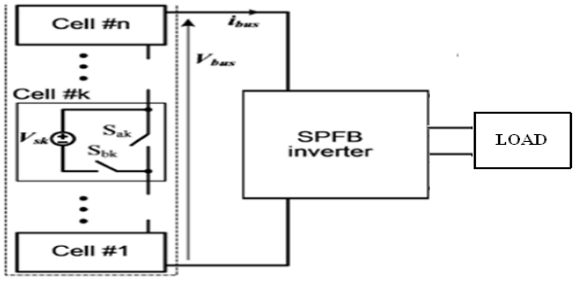

Figure 1 Block diagram of Cascaded H-bridge MLDCL inverter

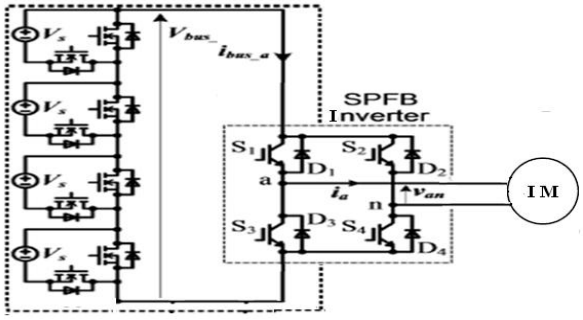

Figure 2 Circuit diagram of Cascaded H -bridge MLDCL inverter

The circuit diagram of the cascaded H-bridge multilevel DC-link inverter topology shown in Figure 2 consists of multilevel DC-link voltage source and single phase full bridge inverter [2].

A. *Multilevel DC-link voltage* source

Multilevel DC-link *voltage* source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two MOSFET switches as shown in the Figure 3. The two MOSFET switches will operate in a toggle fashion [3]. Low on resistance and fast switching capability, low voltage MOSFETS are utilized in each cell source to reduce the inverter cost or to provide a high bandwidth sinusoidal output voltage. The MOSFET switches are triggered by proper switching signals to produce multi level DC-link bus voltage which is indicated by V_{bus} in the circuit diagram.

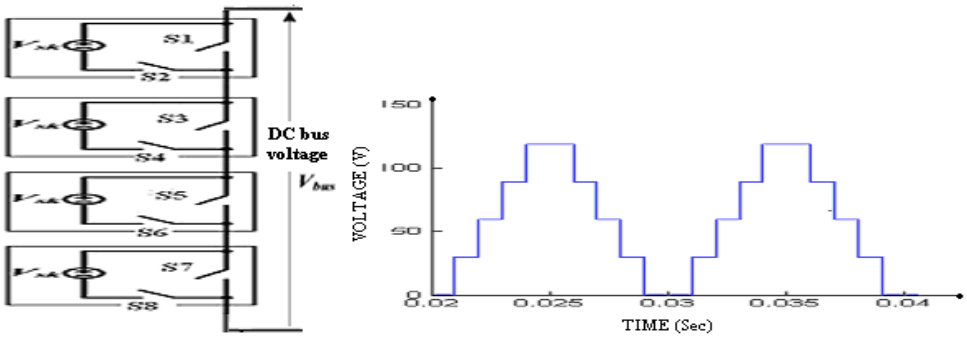

Figure 3 Multilevel DC-link voltage source *and Desired DC bus voltage V_{bus} of cascaded H-bridge MLDCLI*

By giving the switching pulses shown in figure 4 to the switches in four H-bridge cells the MLDCL voltage source produces DC bus voltage V_{bus} with the shape of stair case with (n=4) steps that approximates the rectified waveformof the commanded sinusoidal voltage, where n is the number of cell sources that is given to the SPFB inverter.The desired DC bus voltage V_{bus} is shown in the Figure 5.The switches in four cells will operate at twice of the fundamental frequency of the output voltage [4].

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B. Single phase full bridge inverter

The single phase full bridge (SPFB) inverter shown in Figure 6(a) consists of four IGBT switches S1-S4 which can switch at faster rates and have less demanding gate drive requirements compared to the GTOs in two level inverters [5].

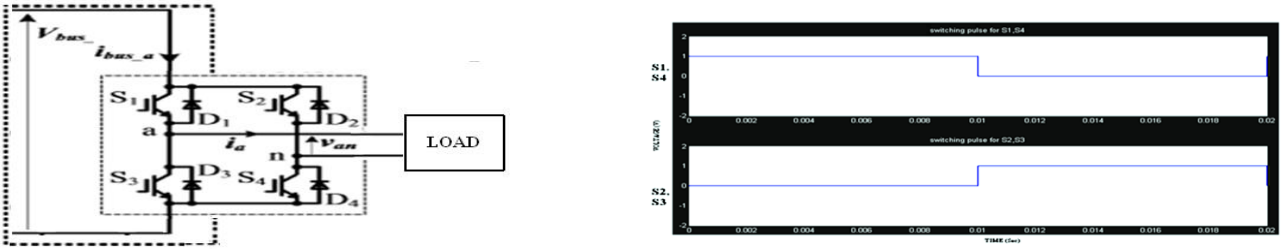

Figure 6(a) Block diagram of SPFB inverter

The switches S1-S4 always work in pairs such that S1&S4 triggered for positive half cycle and S2&S3 will trigger with some delay to produce negative half cycle by operating the switches at the fundamental frequency of the output voltage [6]. The switching sequence for producing multilevel AC output voltage is shown in Figure 6(a).

C. Principle of operation of nine level cascaded H-bridge MLDCL inverter

The principle of operation of nine level cascaded multilevel DC-link inverter is explained by explaining the operating principles of multilevel DC link voltage source and single phase full bridge inverter [7]. To produce nine level AC output voltage V_{an} the multilevel DC-link source is formed by connecting four H-bridge cells in series with each cell having a separate voltage source controlled by two switches S_{ak} and S_{bk} which will operate in a toggle fashion. The cell source is bypassed with S_{ak} on and S_{bk} off, or adds to the DC link bus voltage by reversing the switches. The DC bus voltage V_{bus} is fed to the SPFB inverter [8].

The switching signals shown in Figure 6(b) are given to the SPFB inverter in turn to alternate the voltage polarity of the DC bus voltage V_{bus} for producing an AC output voltage V_{an} of a stair case shape with (2n+1)=9 levels, whose voltages are $-(V_1+V_2+.....+V_n)$, $-(V_1+V_2+.....V_{n-1})$.....,$-V_2$, $-V_1$,0, V_1, V_2,.....$(V_1+V_2+....V_{n-1})$, $(V_1+V_2+....V_n)$. Where V_1, V_2.....V_n are voltages of cell sources. The desired AC output voltage $V_{an\ of}$ cascaded H-bridge is shown in the Figure 6(c) [9].

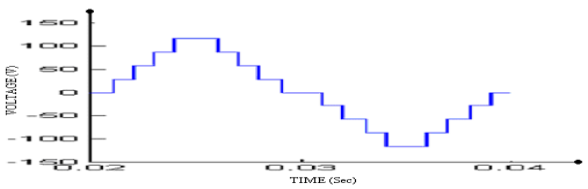

Figure 6(c) Desired AC output voltage V_{an} of cascaded H-bridge MLDCLI

IV. HARDWARE IMPLEMENTATION

The whole circuit can be brought down with dc power supply units, the control circuit, driver circuit and the power circuit. Here the AT89C51 microcontroller is used to generate the triggering pulses to the MOSFETs in the power circuit [10]. The performance of this circuit is evaluated on the basis of low-voltage laboratory scaled-down prototype. An AC voltage of 230V is fed to the power supply circuit comprising 7805, 7812 and 7824 voltage regulator ICs to obtain required dc output voltages. The 5V dc output voltage obtained from regulator IC 7805 is given to the controller circuit and 12V dc output voltage obtained from regulator IC 7812 and 5 v are given to the driver circuit. The 24V DC output

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voltage obtained from regulator IC 78024 is given to the four cells in the power circuit [11]. The control circuit consists of AT89c51 gives the sequence of pulses to be given to the switches in the power circuit. The driver circuit isolates the input from the output and amplifies the pulses to the required level. The power circuit is an arrangement of four cells consists of two MOSFET switches (IRF540) in each cell with an input DC supply of 24V and a SPFB inverter. The gate terminals of the switches are triggered according to the output frequency requirements [12].

The overall circuit diagram of the nine level cascaded H- bridge multilevel dc-link inverter is shown in Figure 11

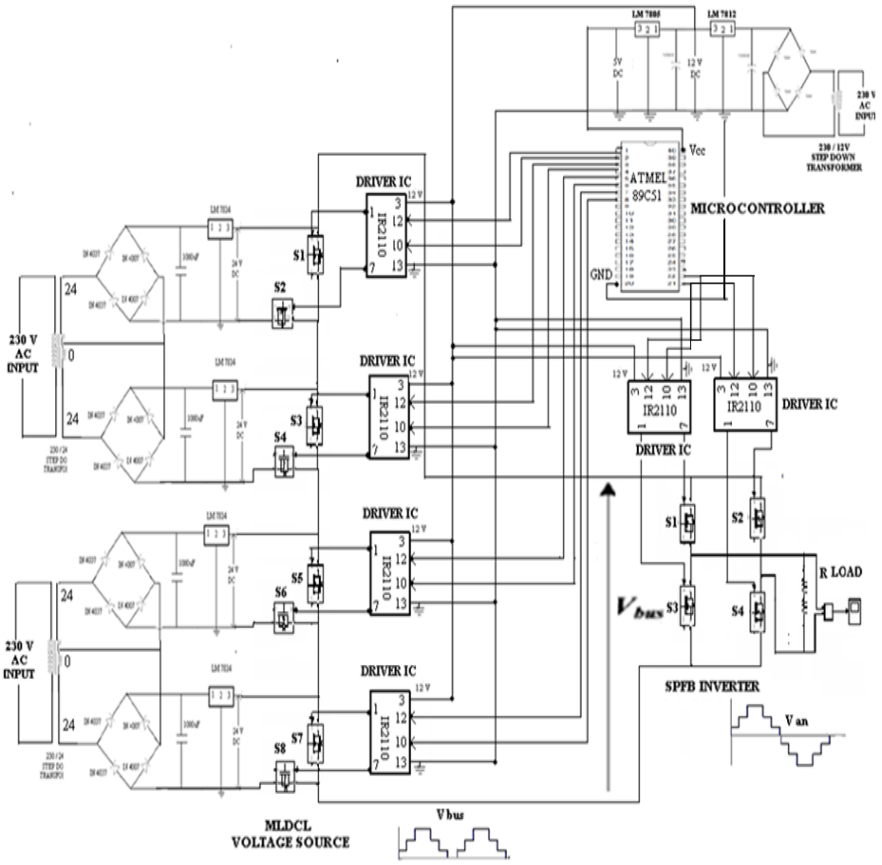

Figure 11 Complete hardware circuit diagram of the cascaded h- bridge multilevel dc-link inverter.

A Power Supply Circuit:

The power supply section of hardware unit is shown in Figure 11(a) the rectifier is given an input voltage of 24 V ac, which is obtained from a step-down transformer [13]. This 24 V ac is converted into dc and regulated by means of regulator IC's 7824 to get +24 V respectively. The output is given to the each cell of the MLDC voltage source.

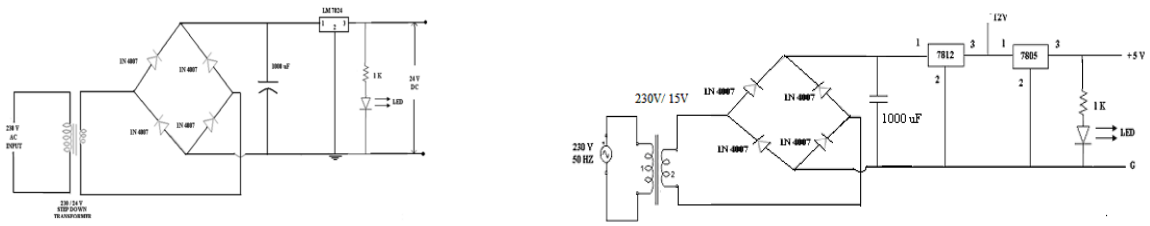

Figure 11(a) DC power supply circuit for each cell of the MLDC voltage source and control and driver circuit

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The rectifier is given an input voltage of 12V ac, which is obtained from a step-down transformer.In figure 11(b) 12V ac is converted into dc and regulated by means of regulator IC's 7812 and 7805 to get +12V and +5V supply which is given as input to driver circuit and microcontroller respectively [14].

B Controller circuit

The controller circuit diagram comprising Micro-Controller Based Pulse-Generating Unit is shown in Figure

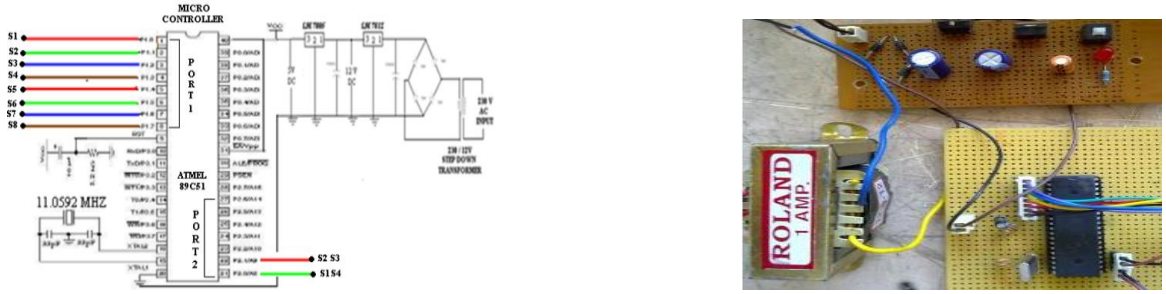

Figure 12(a) Microcontroller circuit

The main part of the hardware circuit is the micro-controller. The line-interfacing unit gives the information about the supply to the micro-controller [15]. A suitable program is written in the micro-controller to generate a train of pulses. In the control circuit an 8 bit microcontroller is used. The driving pulses required for the MOSFETs IRF540 in MLDC voltage source and IRF 840s in the SPFB inverters are obtained from this AT89c51 microcontroller IC. The controller circuit uses a XTAL of frequency 11.0592 MHz .It is connected between pins 18 and 19 which is in turn connected to two 33pFarad capacitor then to ground .pin EA (31) and pin 40 is connected to 5V DC supply from 7805 regulator of power supply circuit.pin 20 is connected to ground. The hard ware circuit of Microcontroller is shown in figure 12(b)

C Driver Circuit:

The driver circuit is used for the purpose of isolation of negative current to the micro-controller, amplification of voltage and to create constant voltage source. The driver circuit diagram is shown in Figure 13(a). The square pulse should have a constant voltage of 5V. This voltage is connected to isolator for isolation purposes. Isolation refers to separation of the power circuit from micro-controller. The 12V DC output voltage obtained from regulator IC 7812 and 5V DC output obtained from 7805 pins are given to 3rd and 9th pins of the driver circuit. When voltage is applied to IR2110 IC, the output voltage will have an increased magnitude that will be sufficient for driving the MOSFET. The pulses from controller will be given to driver's 10th and 12th pins and output is taken from 1st and 7th pin.

The circuit diagram of driver for MLDC voltage source SPFB inverter are shown in Figure13(b)

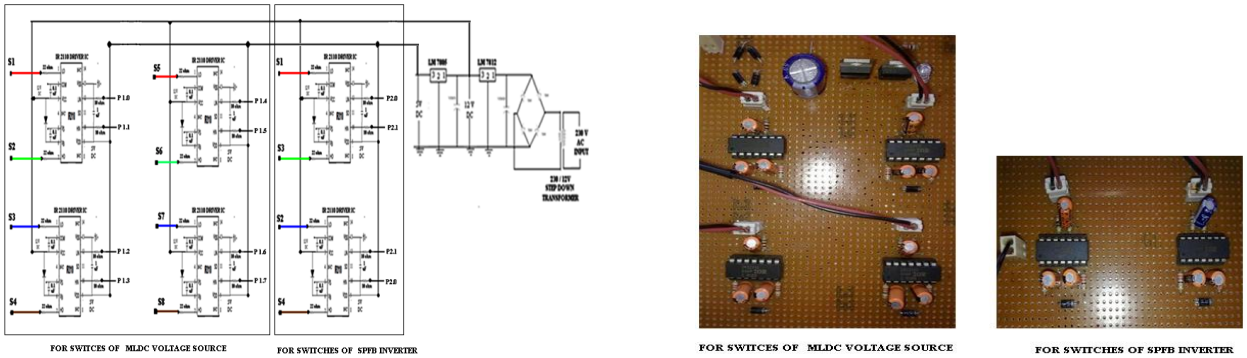

Figure13(b) The hard ware circuit of IR2110 drivers MLDC voltage source SPFB inverter

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D POWER CIRCUIT

Multilevel DC voltage source circuit:

Multilevel DC-link voltage source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two MOSFET switches as shown in the Figure 14(a). The two MOSFET switches will operate in a toggle fashion. The MOSFET switches are triggered by proper switching signals to produce multi level DC-link bus voltage V_{bus}. Multilevel DC-link voltage source consists of 8 switches named S1 –S8. The cell source is bypassed with S1on and S2 off, or adds to the DC link voltage by reversing the switches. Based on this principle the switches in four cells can perform PWM if necessary or switching the switches at twice the fundamental frequency of output voltage. The switching patterns of a controlled switch are given in the Table 2. to produce DC bus voltage V_{bus} with the shape of stair case with (n=4) steps, where n is the number of cell sources.

SWITCH STATE

	SW NO / MODE	S1	S2	S3	S4	S5	S6	S7	S8
0	I	1	0	1	0	1	0	1	0
0.001	II	0	1	1	0	1	0	1	0
0.002	III	0	1	0	1	1	0	1	0
0.003	IV	0	1	0	1	0	1	1	0
0.004	V	0	1	0	1	0	1	0	1
0.006	VI	0	1	0	1	0	1	1	0
0.007	VII	0	1	0	1	1	0	1	0
0.008	VIII	0	1	1	0	1	0	1	0
0.009	IX	1	0	1	0	1	0	1	0
0.01									

1 - ON
0 - OFF

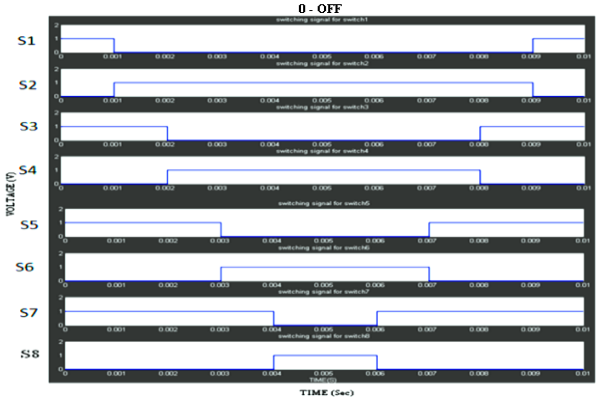

Table 2 Switching sequence of driving signal and Switching pulses for switches in four H-bridge cells

Based on the various modes given in table 1 switching signals are generated for the switches in the half bridge cells. The switching pulses are shown in Figure 4. Table 2 gives the sequence of closure and opening of switches. Based on switching sequence of the switches suitable program has written and burned to the AT89c51 microcontroller for producing triggering pulses for the MOSFETs in the MLDCL voltage source.

The hardware circuit of cell sources in MLDCL voltage sources is shown in figures14(b)

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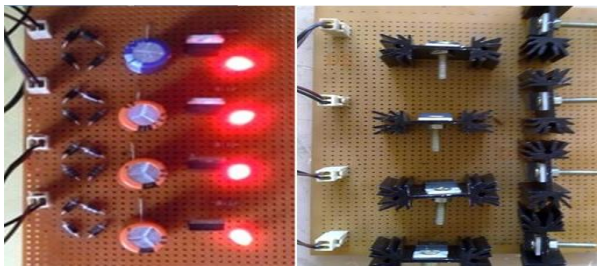


Figure 14(b) Hard ware circuits of cell sources

Figure 15(b) Hardware circuit of SPFB inverter

E Single phase full bridge inverter

Single-phase full-bridge (SPFB) inverter will alternate the polarity of the multilevel DC-link bus voltage to produce an AC voltage of staircase shape. SPFB inverter consists of four MOSFET switches which will always operate in pairs to alternate DC-link bus voltage. The single phase full bridge inverter always operates the all four switches S1-S4 in pairs such that S1&S4 triggered for positive half cycle and S2&S3 will trigger with some delay to produce negative half cycle at the fundamental frequency of the output voltage.

Then SPFB inverter in turn to alternate the voltage polarity for producing an AC voltage V_{an} of a stair case shape with (2n+1)=9 levels, whose voltages are $-(V_1+V_2+.....+V_n)$, $-(V_1+V_2+.....V_{n-1})$.....,$-V_2$, $-V_1$,0, V_1, V_2,.....$(V_1+V_2+....V_{n-1})$, $(V_1+V_2+....V_n)$.. Where V_1, V_2..... V_n are voltages of cell sources. The switching sequence for producing multilevel AC output voltage is shown in Table 3.

SWITCH STATE

	SW NO / MODE	S1	S2	S3	S4
0	I	1	0	0	1
0.01	II	0	1	1	0
0.02					

Table 3 Switching sequence of driving signals of SPFB inverter

The hardware circuit of SPFB inverter is shown in Figure 15(b).

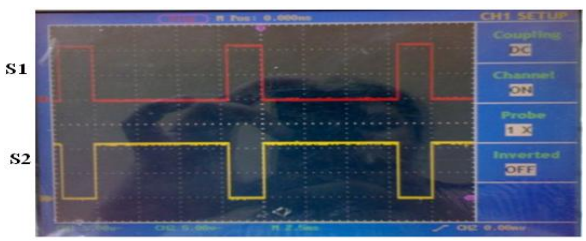
HARDWARE RESULTS

The output waveforms of Microcontroller Circuit, Driver Circuit, output of the inverter with single DC voltage source, multilevel dc voltage source and complete hardware setup are shown in Figure 16(a),16(b), Figure .17(a)17(b),, Figure18,19 and Figure 20 respectively.

B Driver Outputs:

Triggering Pulses For Switches In MLDC Voltage Source Obtained From Driver In DSO are shown in Figure.17 (a)

X-axis 1unit-2.5ms, Y-axis 1unit-5V



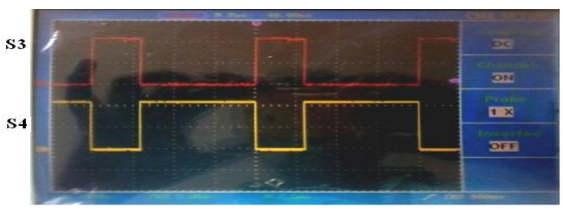


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Figure 17(a) Triggering pulses for switches in MLDC voltage source obtained from driver in DSO

4.5.4 Triggering Pulses for Switches In SPFB Inverter Obtained From Driver In DSO:

X-axis 1unit-2.5ms, Y-axis 1unit-5V

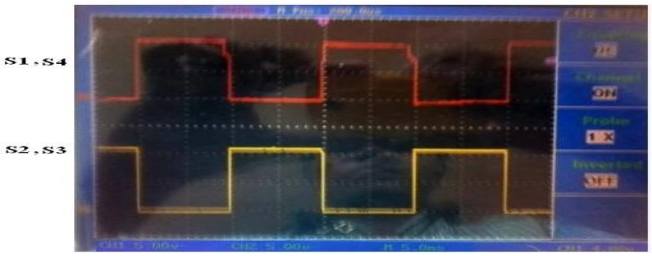
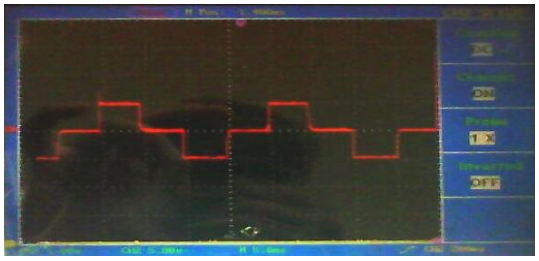


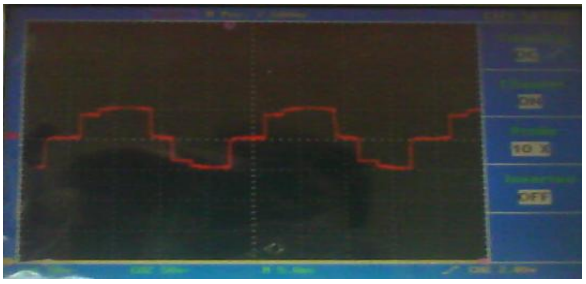
Figure 17(b) Triggering pulses for switches in SPFB inverter obtained from driver in DSO

4.5.5 Output Wave Forms

The out put AC voltage wave form of 50 Hz frequency of the SPFB inverter with single DC voltage source as input is shown in Figure 18

X-axis 1unit-5ms, Y-axis 1unit-5V





X-axis 1unit-5ms, Y-axis 1unit-20V

Figure 18 Output of the inverter with single DC voltage source

Figure no 19 Output of the inverter with single DC voltage source

The out put AC voltage wave form of 50 Hz frequency of the multilevel DC link inverter with 4 DC voltage cell sources as input is shown in Figure 19

The over all hardware setup for nine level cascaded H-bridge MLDCL inverter supplying R load is shown in figure

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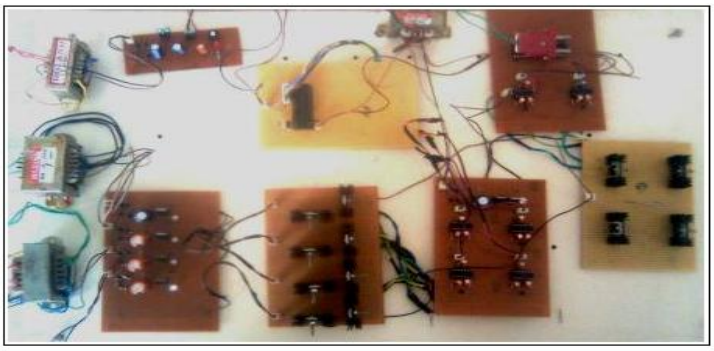

Figure 20Complete Hardware Setup

D. Comparison of the nine level cascade MLDCL Inverter and the existing MLI

From the previous discussions, it is demonstrated that the MLDCL inverters can significantly reduce the component count. Fig.21 plots a chart for comparison of the required number of switches between the proposed MLDCL inverter and the cascaded H-bridge counterpart. As the number of voltage levels m grows, the number of active switches required is 2*(m-1) =16 for existing cascaded multilevel inverter and m+3 =12 switches are required for cascaded H-bridge MLDCL inverter[8]

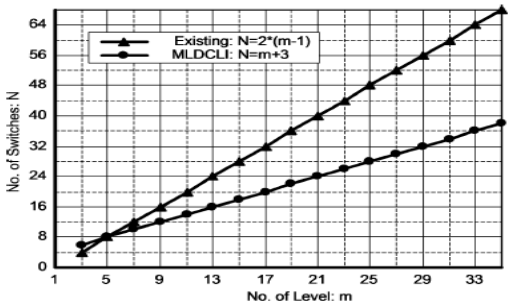

Figure. 21. Comparison of required number of switches.

V. CONCLUSION

The presented nine level cascaded H-bridge MLDCL inverters can eliminate roughly half the number of switches, their gate drivers compared with the existing cascaded MLI counterparts. Despite a higher total VA rating of the switches, the cascaded MLDCL inverters are cost less due to the savings from the eliminated gate drivers and from fewer assembly steps because of the substantially reduced number of components, which also leads to a smaller size and volume.

The principle of operation of nine level cascaded H-bridge MLDCL inverter for supplying R load is presented. The experimentally generated waveforms of gate pulses from controller and driver for triggering switches of MLDC voltage source and SPFB inverter are presented and the complete hardware of nine level cascaded H-bridge MLDCL inverter with output voltage wave forms of frequency 50HZ of for supplying R load is implemented with ATMEL 89C51 microcontroller.

One application area in the low-power range (≤ 100 kW) for the MLDCL inverters is in permanent-magnet (PM) motor drives employing a PM motor of very low inductance.The MLDCL inverter can utilize the fast-switching low-cost low-voltage MOSFETs in the half-bridge cells, and the IGBT's in the single-phase bridges to dramatically reduce current and torque ripples and to improve motor efficiency by reducing the associated copper and iron losses resulting from the current ripple. These configurations may also be applied in distributed power generation involving fuel cells and photovoltaic cells.

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